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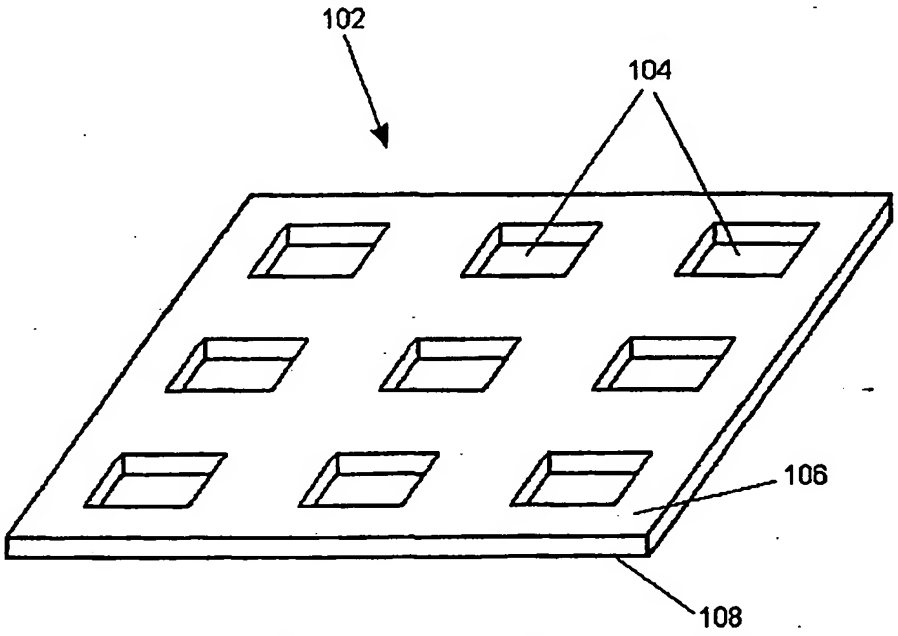
(54) Title: MICROELECTRONIC SUBSTRATE WITH INTEGRATED DEVICES



(57) Abstract: A microelectronic substrate including at least one microelectronic die disposed within an opening in a microelectronic substrate core, wherein an encapsulation material is disposed within portions of the opening not occupied by the microelectronic dice, or a plurality microelectronic dice encapsulated without the microelectronic substrate core. Interconnection layers of dielectric materials and conductive traces are then fabricated on the microelectronic die, the encapsulation material, and the microelectronic substrate core (if present) to form the microelectronic substrate.

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MICROELECTRONIC SUBSTRATE WITH INTEGRATED DEVICES

BACKGROUND OF THE INVENTION

Related Applications: This is a continuation-in-part of application No. 09/640961, filed August 16, 2000.

Field of the Invention: The present invention relates to apparatus and processes for the fabrication of a microelectronic substrate. In particular, the present invention relates to a fabrication technology that encapsulates at least one microelectronic die within a microelectronic substrate core or that encapsulates at least one microelectronic die (without a microelectronic substrate core) to form a microelectronic substrate.

State of the Art: Substrates which connect individual microelectronic devices exist in virtually all recently manufactured electronic equipment. These substrates are generally printed circuit boards. Printed circuit boards are basically dielectric substrates with metallic traces formed in or upon the dielectric substrate. One type of printed circuit board is a single-sided board. As shown in FIG. 20, single-sided board 200 consists of a dielectric substrate 202, such as an FR4 material, epoxy resins, polyimides, triazine resins, and the like, having conductive traces 204, such as copper, aluminum, and the like, on one side (i.e., first surface 206), wherein the conductive traces 204 electrically interconnect microelectronic devices 208 (shown as flip-chips) attached to the first surface 206. However, single-sided boards 200 result in relatively long conductive traces 204 which, in turn, results in slower speeds and performance. Single-sided boards 200 also require substantial surface area for the routing of the conductive traces 204 to interconnect the various microelectronic devices 208 which increases the size of the resulting assembly.

It is, of course, understood that the depiction of the dielectric substrate 202, the conductive traces 204, and the microelectronic devices 208 in FIG. 20 (and subsequently FIGs. 21 and 22) are merely for illustration purposes and certain dimensions are greatly exaggerated to show the concept, rather than accurate details thereof.

Double-sided boards 210 were developed to help alleviate the problem with relatively long conductive traces. As shown in FIG. 21, the double-sided board 210 comprises a dielectric substrate 202 having conductive traces 204 on the dielectric substrate first surface 206 and on a dielectric substrate second surface 212. At least one electrically conductive via 214 extends through the dielectric substrate 202 to connect at least one conductive trace 204 on the first surface 206 with at least one conductive trace 204 on the second surface 212. Thus, the microelectronic devices 208 on the dielectric substrate first surface 206 and on the dielectric substrate second surface 212 may be in electrical communication. The electrically conductive vias 214 are generally plated through-hole vias and may be formed in any manner known in the art.

FIG. 22 illustrates another board design, known as a multi-layer board 220. A multi-layer board 220 comprises two or more pieces of dielectric material (shown as first dielectric material 222 and second dielectric material 224) with conductive traces 204 thereon and therebetween with electrically conductive vias 214 formed through the first dielectric material 222 and the second dielectric material 224. This design allows for shorter traces and reduced surface area requirements for conductive trace 204 routing.

Although such boards have been adequate for past and current microelectronic device applications, the need for higher performance and shorter traces of substrate boards increases as the speed and performance of the microelectronic devices increases.

Therefore, it would be advantageous to develop new substrates/boards, which achieve higher speed and performance.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIG. 1 is an oblique view of a microelectronic substrate core, according to the present invention;

FIG. 2 is a top plan view of a microelectronic substrate core having examples of alternate microelectronic substrate core openings, according to the present invention;

FIG. 3 is a side cross-sectional view of a microelectronic substrate core abutted to a protective film, according to the present invention;

FIG. 4 is a side cross-sectional view of microelectronic dice disposed within openings of the microelectronic substrate core, which also abuts the protective film, according to the present invention;

FIG. 5 is a side cross-sectional view of the assembly of FIG. 4 after encapsulation, according to the present invention;

FIG. 6 is a side cross-sectional view of the assembly of FIG. 5 after the protective film has been removed, according to the present invention;

FIGs. 7-15 are side cross-sectional views of a process of forming interconnection layers on a microelectronic die, encapsulation material, and a microelectronic substrate core, according to the present invention;

FIG. 16 is a side cross-sectional view of the assembly of FIG. 6 having interconnection layers and solder balls positioned thereon, according to the present invention;

FIG. 17 is a side cross-sectional view of the assembly of FIG. 16 without a microelectronic substrate core, according to the present invention;

FIG. 18 is a side cross-sectional view of microelectronic dice and devices of varying sizes;

FIG. 19 is a side cross-sectional view of multiple microelectronic dice within a single core opening;

FIG. 20 is a cross-sectional view of a single-sided board, as known in the art;

FIG. 21 is a cross-sectional view of a double-sided board, as known in the art; and

FIG. 22 is a cross-sectional view of a multi-layer board, as known in the art.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Although FIGs. 1-19 illustrate various views of the present invention, these figures are not meant to portray microelectronic assemblies in precise detail. Rather, these figures illustrate microelectronic assemblies in a manner to more clearly convey the concepts of the present invention. Additionally, elements common between the figures retain the same numeric designation.

The present invention includes a substrate fabrication technology that places at least one microelectronic die within at least one opening in a microelectronic substrate core and secures the microelectronic die/dice within the opening(s) with an encapsulation material or that encapsulates at least one microelectronic die within an encapsulation material without a microelectronic substrate core. Interconnection layers

of dielectric materials and conductive traces are then fabricated on the microelectronic die/dice, the encapsulation material, and the microelectronic substrate core (if present) to form a microelectronic substrate. The term "microelectronic substrate" is defined to include motherboards, peripheral cards, cartridges, multi-chip module substrates, and similar structures as will be evident to one skilled in the art.

The technical advantage of this invention is that it enables the microelectronic substrate to be built around the microelectronic die/dice, which results in a shorter interconnect distance between microelectronic dice within the microelectronic substrate and microelectronic devices attached thereto. This, in turn, results in higher speed and performance. Furthermore, the microelectronic substrate of the present invention may also result in a smaller form factor, which is well suited to mobile systems (i.e., laptop computers, handheld devices, personal digital assistants, etc.).

FIG. 1 illustrates a microelectronic substrate core 102 used to fabricate a microelectronic substrate. The microelectronic substrate core 102 preferably comprises a substantially planar material. The material used to fabricate the microelectronic substrate core 102 may include, but is not limited to, a Bismaleimide Triazine ("BT") resin based laminate material, an FR4 laminate material (a flame retarding glass/epoxy material), various polyimide laminate materials, ceramic material, and the like, and metallic materials (such as copper) and the like. The microelectronic substrate core 102 has at least one opening 104 extending therethrough from a first surface 106 of the microelectronic substrate core 102 to an opposing second surface 108 of the microelectronic substrate core 102. As shown in FIG. 2, the opening(s) 104 may be of any shape and size including, but not limited to, rectangular/square 104a, rectangular/square with rounded corners 104b, and circular 104c. The only limitation on

the size and shape of the opening(s) 104 is that they must be appropriately sized and shaped to house a corresponding microelectronic die or dice therein, as will be discussed below.

FIG. 3 illustrates the microelectronic substrate core first surface 106 abutting a protective film 112. The protective film 112 is preferably a substantially flexible material, such as Kapton® polyimide film (E. I. du Pont de Nemours and Company, Wilmington, Delaware), but may be made of any appropriate material, including metallic films. In a preferred embodiment, the protective film 112 would have substantially the same coefficient of thermal expansion (CTE) as the microelectronic substrate core. FIG. 4 illustrates microelectronic dice 114, each having an active surface 116 and a back surface 118, placed in corresponding openings 104 of the microelectronic substrate core 102. The microelectronic dice 114 may be any known active or passive microelectronic device including, but not limited to, logic (CPUs), memory (DRAM, SRAM, SDRAM, etc.), controllers (chip sets), capacitors, resistors, inductors, and the like.

In a preferred embodiment (illustrated), the thickness 117 of the microelectronic substrate core 102 and the thickness 115 of the microelectronic dice 114 are substantially equal. The microelectronic dice 114 are each placed such that their active surfaces 116 abut the protective film 112. The protective film 112 may have an adhesive, such as silicone or acrylic, which attaches to the microelectronic substrate core first surface 106 and the microelectronic die active surface 116. This adhesive-type film may be applied prior to placing the microelectronic die 114 and microelectronic substrate core 102 in a mold, liquid dispense encapsulation system (preferred), or other piece of equipment used for the encapsulation process. The protective film 112 may

also be a non-adhesive film, such as a ETFE (ethylene - tetrafluoroethylene) or Teflon® film, which is held on the microelectronic die active surface 116 and the microelectronic substrate core first surface 106 by an inner surface of the mold or other piece of equipment during the encapsulation process.

The microelectronic die 114 is then encapsulated with an encapsulation material 122, such as plastics, resins, epoxies, elastomeric (e.g., rubbery) materials, and the like. As shown in FIG. 5, the encapsulation material 122 is disposed in portions of the opening(s) 104 not occupied by the microelectronic die 114. The encapsulation of the microelectronic die 114 may be achieved by any known process, including but not limited to transfer and compression molding, and dispensing. The encapsulation material 122 secures the microelectronic die 114 within the microelectronic substrate core 102 and provides mechanical rigidity for the resulting structure and provides surface area for the subsequent build-up of trace layers.

After encapsulation, the protective film 112 is removed, as shown in FIG. 6, to expose the microelectronic die active surface 116. As also shown in FIG. 6, the encapsulation material 122 is preferably molded or dispensed to fill the space between the microelectronic substrate core first surface 106 and the microelectronic die active surface 116. This results in at least one surface 124 that is substantially planar to the microelectronic die active surface 116 and the microelectronic substrate core first surface 106. The encapsulation material surface 124 may be utilized in further fabrication steps, along with the microelectronic substrate core first surface 106, as additional surface area for the formation of interconnection layers, such as dielectric material layers and conductive traces.

Although the following description relates to a bumpless, built-up layer technique for the formation of interconnection layers, the method of fabrication is not so limited. The interconnection layers may be fabricated by a variety of techniques known in the art.

FIG. 7 illustrates a view of a single microelectronic die 114 encapsulated with encapsulation material 122 within the microelectronic substrate core 102. The microelectronic die 114, of course, includes a plurality of electrical contacts 132 located on the microelectronic die active surface 116. The electrical contacts 132 are electrically connected to circuitry (not shown) within the microelectronic die 114. Only four electrical contacts 132 are shown for sake of simplicity and clarity.

As shown in FIG. 8, a first dielectric layer 136, such as epoxy resin, polyimide, bisbenzocyclobutene, and the like, is disposed over the microelectronic die active surface 116 (including the electrical contacts 132), the microelectronic substrate core first surface 106, and the encapsulation material surface 124. The dielectric layers of the present invention are preferably filled epoxy resins available from Ibiden U.S.A. Corp., Santa Clara, California, U.S.A. and from Ajinomoto U.S.A., Inc., Paramus, New Jersey, U.S.A. The formation of the first dielectric layer 136 may be achieved by any known process, including but not limited to lamination, spin coating, roll coating, and spray-on deposition.

As shown in FIG. 9, a plurality of vias 138 are then formed through the first dielectric layer 136. The plurality of vias 138 may be formed by any method known in the art, including but not limited to laser drilling, photolithography (usually followed by an etch), and, if the first dielectric layer 136 is photoactive, forming the plurality of vias

138 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

A plurality of conductive traces 142 is formed on the first dielectric layer 136, as shown in FIG. 10, wherein a portion of each of the plurality of conductive traces 142 extends into at least one of said plurality of vias 138 (see FIG. 9) to make electrical contact with the contacts 132. The plurality of conductive traces 142 may be made of any applicable conductive material, such as copper, aluminum, and alloys thereof.

The plurality of conductive traces 142 may be formed by any known technique, including but not limited to semi-additive plating and photolithographic techniques. An exemplary semi-additive plating technique can involve depositing a seed layer, such as a sputter-deposited or electroless-deposited metal on the first dielectric layer 136. A resist layer is then patterned on the seed layer, such as a titanium/copper alloy, followed by electrolytic plating of a layer of metal, such a copper, on the seed layer exposed by open areas in the patterned resist layer. The patterned resist layer is stripped and portions of the seed layer not having the layer of metal plated thereon is etched away. Other methods of forming the plurality of conductive traces 142 will be apparent to those skilled in the art.

As shown in FIG. 11, a second dielectric layer 144 is disposed over the plurality of conductive traces 142 and the first dielectric layer 136. The formation of the second dielectric layer 144 may be achieved by any known process, including but not limited to film lamination, spin coating, roll coating, and spray-on deposition.

As shown in FIG. 12, a plurality of second vias 146 is then formed through the second dielectric layer 144. The plurality of second vias 146 may be formed any method known in the art, including but not limited to laser drilling and, if the second dielectric

layer 144 is photoactive, forming the plurality of second vias 146 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

If the plurality of conductive traces 142 is not capable of placing the plurality of second vias 146 in an appropriate position, then other portions of the conductive traces are formed in the plurality of second vias 146 and on the second dielectric layer 144, another dielectric layer formed thereon, and another plurality of vias is formed in the dielectric layer, such as described in FIGs. 10–12. The layering of dielectric layers and the formation of conductive traces can be repeated until the vias are in an appropriate position, and sufficient electrical connectivity is established to enable the required electrical performance. Thus, portions of a single conductive trace be formed from multiple portions thereof and can reside on different dielectric layers.

A second plurality of conductive traces 148 may be formed, wherein a portion of each of the second plurality of conductive traces 148 extends into at least one of said plurality of second vias 146. The second plurality of conductive traces 148 each includes a landing pad 150 (an enlarged area on the traces demarcated by a dashed line 152), as shown in FIG. 13.

Once the second plurality of conductive traces 148 and landing pads 150 are formed, they can be used in the formation of conductive interconnects, such as solder bumps, solder balls, pins, and the like, for communication with external components (not shown). For example, a solder mask material 156 can be disposed over the second dielectric layer 144 and the second plurality of conductive traces 154 and landing pads 150. A plurality of vias 158 is then formed in the solder mask material 156 to expose at least a portion of each of the landing pads 150, as shown in FIG. 14. A plurality of conductive bumps 160, such as solder bumps, can be formed, if desired, such as by, but

not limited to, screen printing solder paste followed by a reflow process or by known plating techniques, on the exposed portion of each of the landing pads 154, as shown in FIG. 15.

FIG. 16 illustrates a plurality of microelectronic dice 114 encapsulated with encapsulation material 122 within the microelectronic substrate core 102 to form the microelectronic substrate 170 of the present invention. At least one interconnection layer is formed on the microelectronic dice active surfaces 116, the microelectronic substrate core first surface 106, and the encapsulation material surface 124 in the manner previously discussed. The layer(s) of dielectric material and conductive traces comprising the interconnection layer is simply designated together as interconnection layer 162 in FIG. 16. This interconnection layer 162 serves not only to form connections between the microelectronic dice 114 and the plurality of conductive bumps 160, as described above, but also to allow electrical communication among the microelectronic dice 114 disposed within the microelectronic substrate core 102.

Once the interconnection layer 162 is formed, at least one microelectronic device 164 may be attached to a top surface 166 of the interconnection layer 162 by the conductive bumps 160. The conductive bumps 160 active electrical communication between at least one microelectronic device 164 and at least one microelectronic die 114. It is, of course, understood that the conductive bumps 160 may be formed on the interconnection layer 162 (as shown in FIG. 15) or on the microelectronic device 164. It is also understood that, although FIG. 16 illustrates the microelectronic devices 164 as packaged flip-chips, the microelectronic devices may be any known active or passive microelectronic devices 164 including, but not limited to, logic (CPUs), memory (DRAM, SRAM, SDRAM, etc.), controllers (chip sets), capacitors, resistors, and the

like. Furthermore, in addition to flip-chip attachment, as illustrated in FIG. 16, attachment of the microelectronic devices 164 may be accomplished by other methods, such as wirebonding or other methods known to those skilled in the art.

FIG. 17 illustrates the assembly of FIG. 16 wherein the microelectronic substrate 180 is fabricated without the microelectronic substrate core 102 (see FIG. 16) in a similar manner as described for the microelectronic substrate 170 (see FIG. 16).

As illustrated in FIG. 18, the microelectronic dice 114 and the microelectronic devices 164 may be a variety of sizes and shapes. Furthermore, as illustrated in FIG. 19, a plurality of microelectronic dice 114 may be disposed in a single opening in the microelectronic substrate core 102. This configuration allows interacting microelectronic dice 114 to communicate with one another to be as close as possible to improve electrical performance by shortening conductive trace (not shown) lengths therebetween, as will be understood by those skilled in the art.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A microelectronic substrate, comprising:

a microelectronic substrate core having a first surface and an opposing second surface, said microelectronic substrate core having at least one opening defined therein extending from said microelectronic substrate core first surface to said microelectronic substrate core second surface;

at least one microelectronic die disposed within said at least one opening, said at least one microelectronic die having an active surface; and

an encapsulation material adhering said microelectronic substrate core to said at least one microelectronic die.

2. The microelectronic substrate of claim 1, wherein said encapsulation material further includes at least one surface substantially planar to said microelectronic die active surface and said microelectronic substrate core first surface.

3. The microelectronic substrate of claim 2, further including interconnection layers disposed on at least one of said microelectronic die active surface, said at least one encapsulation material surface, and said microelectronic substrate core first surface.

4. The microelectronic substrate of claim 3, further including at least one microelectronic device attached to said interconnection layers.

5. The microelectronic substrate of claim 3, wherein said interconnection layers comprise at least one dielectric layer abutting at least one of said microelectronic die active surface, said at least one encapsulation material surface, and said microelectronic substrate core first surface and at least one conductive trace disposed on said at least one dielectric layer.

6. The microelectronic substrate of claim 5, wherein said at least one conductive trace extends through said at least one dielectric layer to contact at least one electrical contact on said microelectronic die active surface.

7. The microelectronic substrate of claim 1, wherein said microelectronic substrate core is selected from the group consisting of bismaleimide triazine resin based laminate material, an FR4 laminate material, polyimide laminates, ceramics, and metals.

8. A microelectronic substrate, comprising:

a plurality microelectronic dice each having an active surface; and

an encapsulation material disposed at least between each of said plurality of microelectronic dice wherein said active surface of each of said plurality of microelectronic dice is exposed.

9. The microelectronic substrate of claim 8, wherein said encapsulation material further includes at least one surface substantially planar to each of said plurality of microelectronic die active surfaces.

10. The microelectronic substrate of claim 9, further including interconnection layers disposed on at least one of said plurality of microelectronic die active surfaces and said at least one encapsulation material surface.

11. The microelectronic substrate of claim 10, further including at least one microelectronic device attached to said interconnection layers.

12. The microelectronic substrate of claim 10, wherein said interconnection layers comprise at least one dielectric layer abutting at least one of said microelectronic die active surface and said at least one encapsulation material surface; and at least one conductive trace disposed on said at least one dielectric layer.

13. The microelectronic substrate of claim 12, wherein said at least one conductive trace extends through said at least one dielectric layer to contact at least one electrical contact on said microelectronic die active surface.

14. A method of fabricating a microelectronic substrate, comprising:

providing a microelectronic substrate core having a first surface and an opposing second surface, said microelectronic substrate core having at least one opening defined therein extending from said microelectronic substrate core first surface to said microelectronic substrate core second surface;

disposing at least one microelectronic die within said at least one opening, said at least one microelectronic die having an active surface; and

adhering said microelectronic substrate core to said at least one microelectronic die with an encapsulation material.

15. The method of claim 14, wherein adhering said microelectronic substrate core to said at least one microelectronic with said encapsulation material further includes forming at least one encapsulation material surface substantially planar to said microelectronic die active surface and said microelectronic substrate core first surface.

16. The method of claim 15, further including forming interconnection layers on said encapsulation material surface, said microelectronic die active surface and said microelectronic substrate core first surface.

17. The method of claim 16, further including electrically attaching at least one microelectronic device to a top surface of said interconnection layers.

18. The method of claim 16, wherein forming interconnection layers comprises:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface, said at least one encapsulation material surface, and said microelectronic substrate core first surface;

forming at least one via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said at least one via to electrically contact said microelectronic die active surface.

19. The method of claim 18, further including forming at least one additional dielectric material layer disposed over said at least one conductive trace and said at least one dielectric material layer.

20. The method of claim 19, further including forming at least one additional conductive trace to extend through and reside on said at least one additional dielectric material layer.

21. The method of claim 14, wherein said providing said microelectronic substrate core comprises providing a microelectronic substrate core selected from the group consisting of bismaleimide triazine resin based laminate material, an FR4 laminate material, polyimide laminates, ceramics, and metals.

22. The method of claim 14, further including abutting said microelectronic substrate core first surface and said microelectronic die active surface against a protective film prior to adhering said microelectronic substrate core to said at least one microelectronic die with an encapsulation material.

23. The method of claim 22, wherein abutting said microelectronic substrate core first surface and said microelectronic die active surface against a protective film

comprises abutting said microelectronic substrate core first surface and said microelectronic die active surface against an adhesive layer on said protective film prior to adhering said microelectronic substrate core to said at least one microelectronic die with an encapsulation material.

24. A method of fabricating a microelectronic substrate, comprising:

providing a protective film;

abutting active surfaces of a plurality of microelectronic dice against said protective film;

disposing an encapsulation material at least between each of said plurality of microelectronic dice; and

removing said protective film.

25. The method of claim 24, wherein disposing said encapsulation material includes forming at least one encapsulation material surface substantially planar to said microelectronic die active surface.

26. The microelectronic substrate of claim 25, further including forming interconnection layers on at least one of said plurality of microelectronic die active surfaces and said at least one encapsulation material surface.

27. The method of claim 26, further including electrically attaching at least one microelectronic device to a top surface of said interconnection layers.

28. The method of claim 26, wherein forming interconnection layers comprises:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface and said at least one encapsulation material surface;

forming at least one via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said at least one via to electrically contact said microelectronic die active surface.

29. The method of claim 28, further including forming at least one additional dielectric material layer disposed over said at least one conductive trace and said at least one dielectric material layer.

30. The method of claim 29, further including forming at least one additional conductive trace to extend through and reside on said at least one additional dielectric material layer.

31. The method of claim 24, wherein providing said protective film includes providing said protective film having an adhesive thereon; and wherein abutting active surfaces of a plurality of microelectronic dice against said protective film comprises abutting active surfaces of a plurality of microelectronic dice against said adhesive of said protective film.

FIG. 1

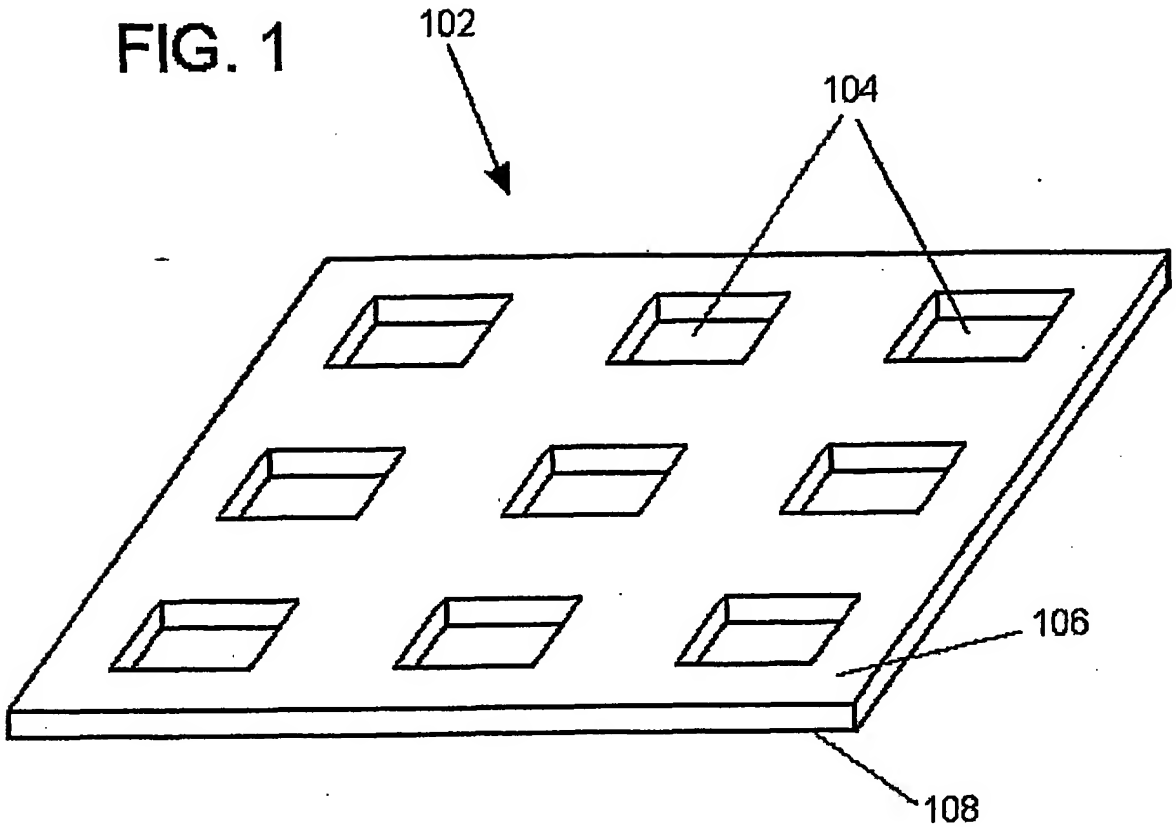


FIG. 3

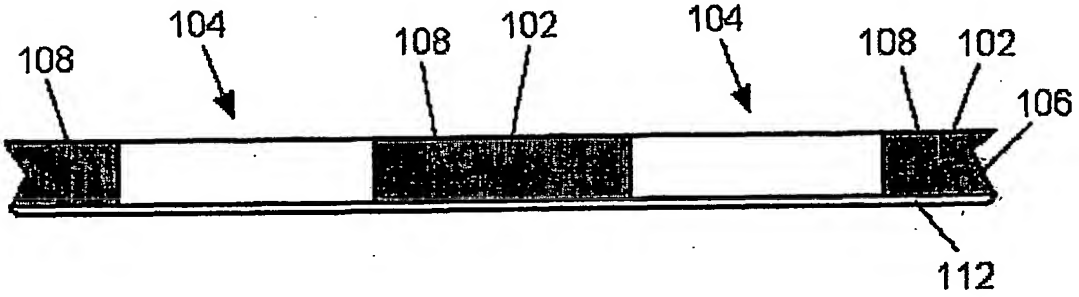


FIG. 2

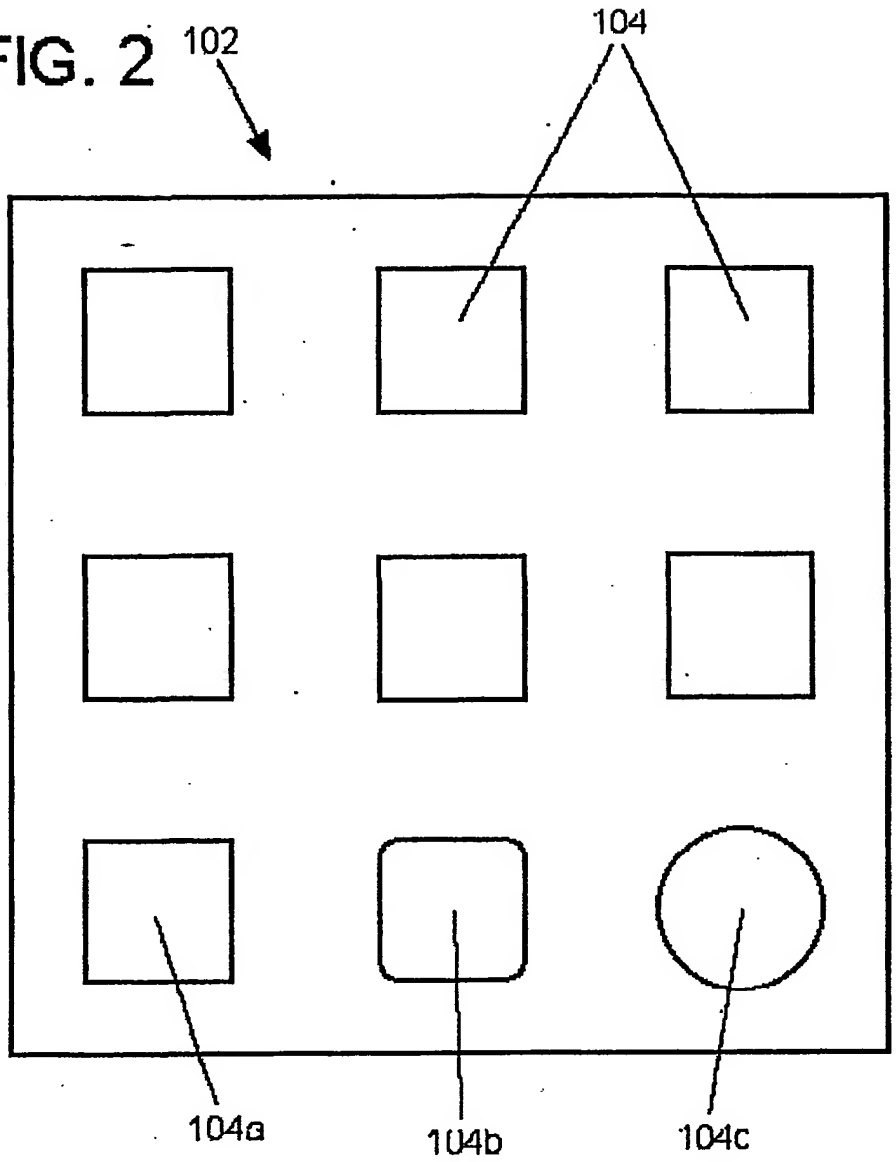


FIG. 4

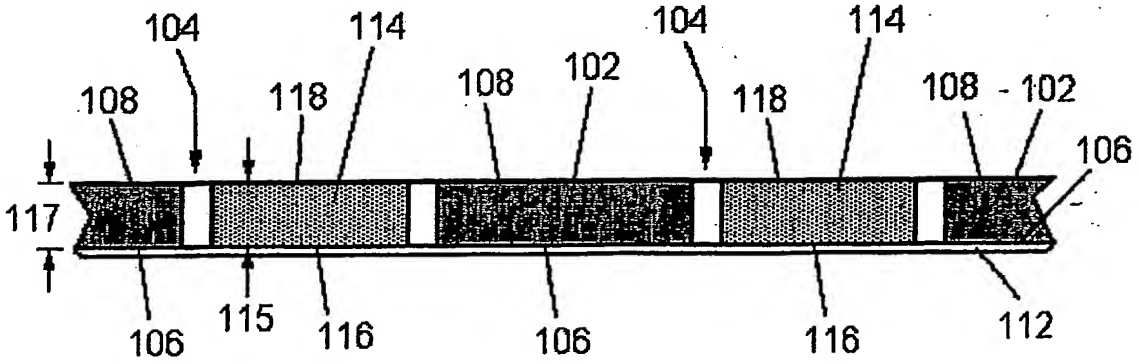


FIG. 5

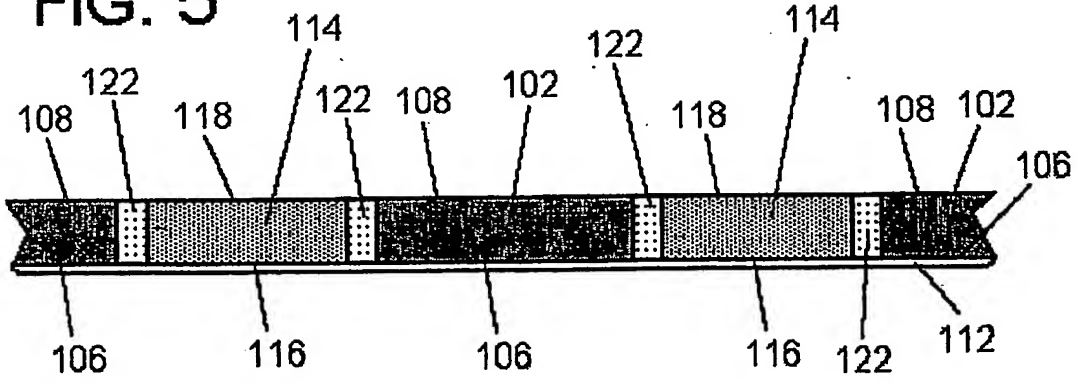


FIG. 6

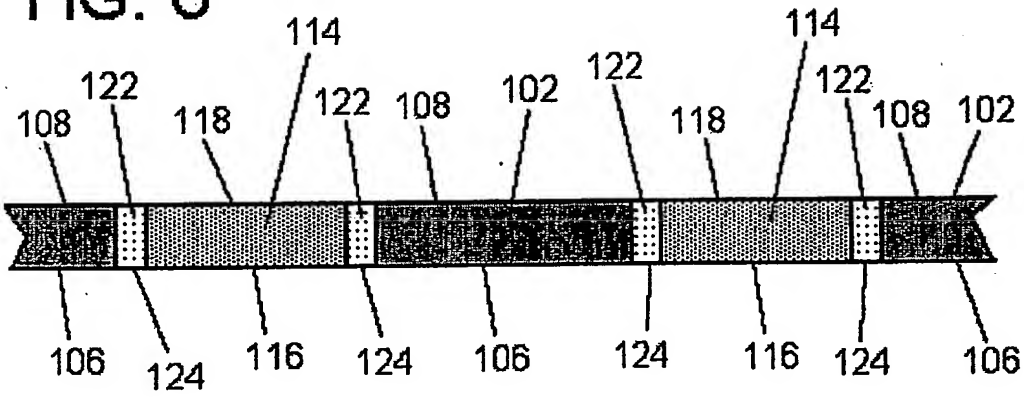


FIG. 7

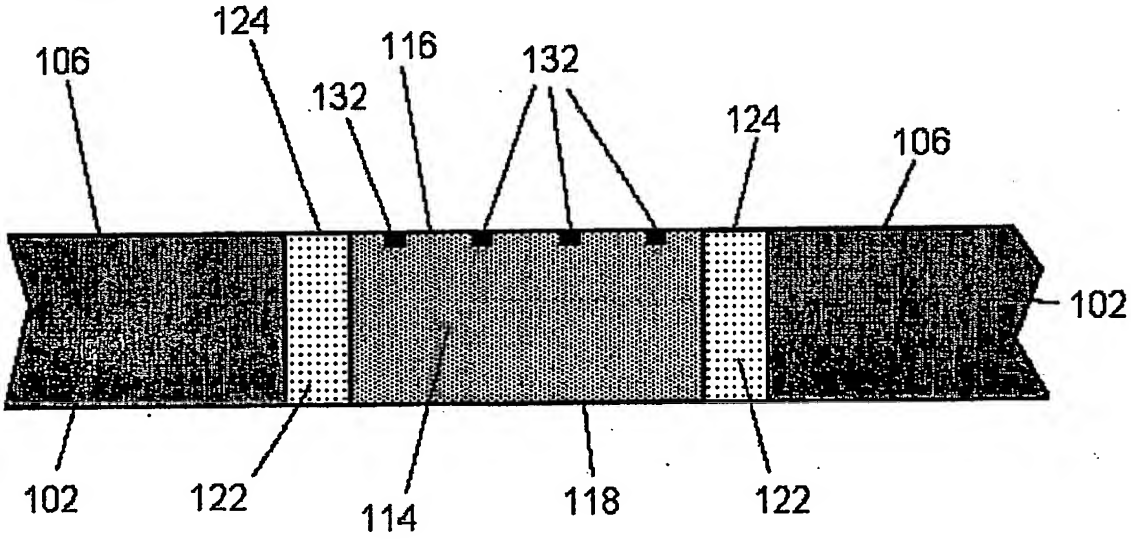


FIG. 8

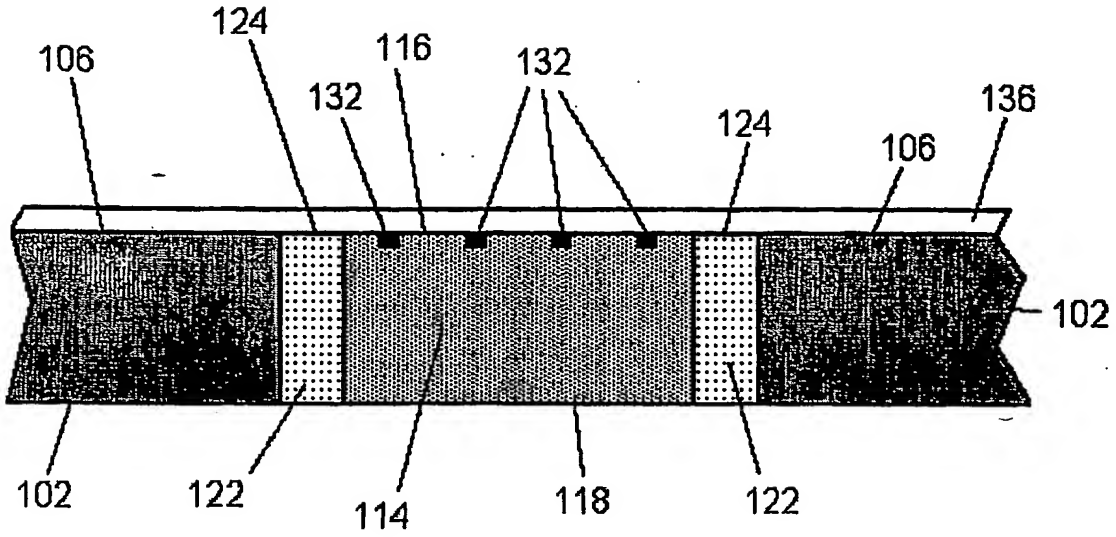


FIG. 9

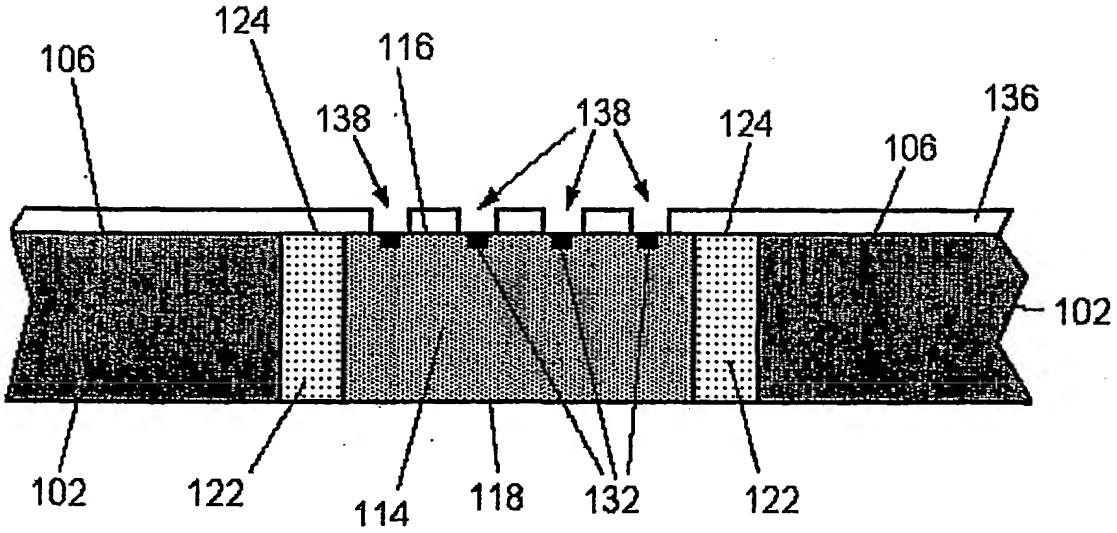


FIG. 10

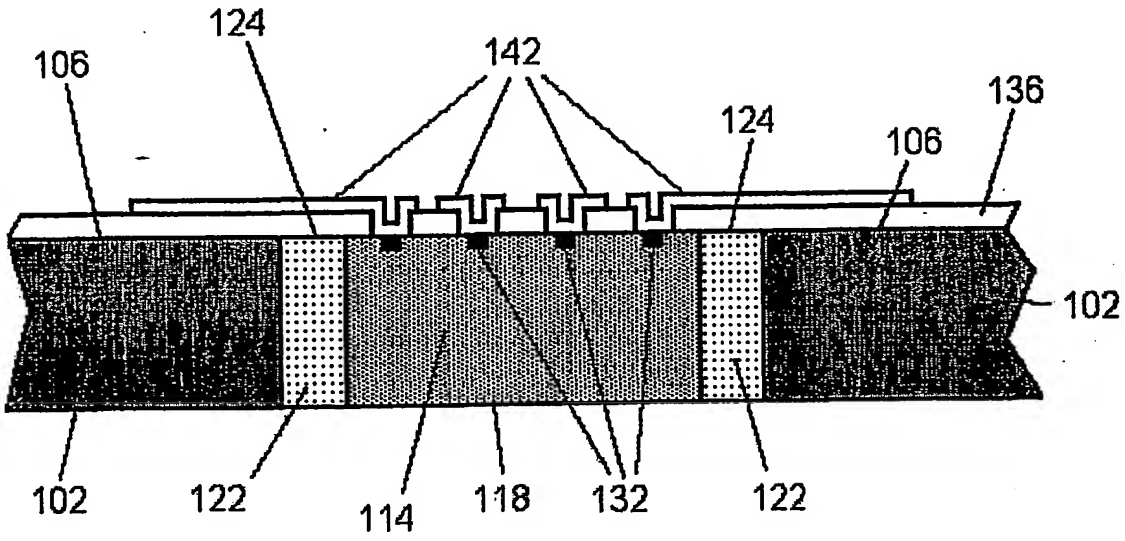


FIG. 11

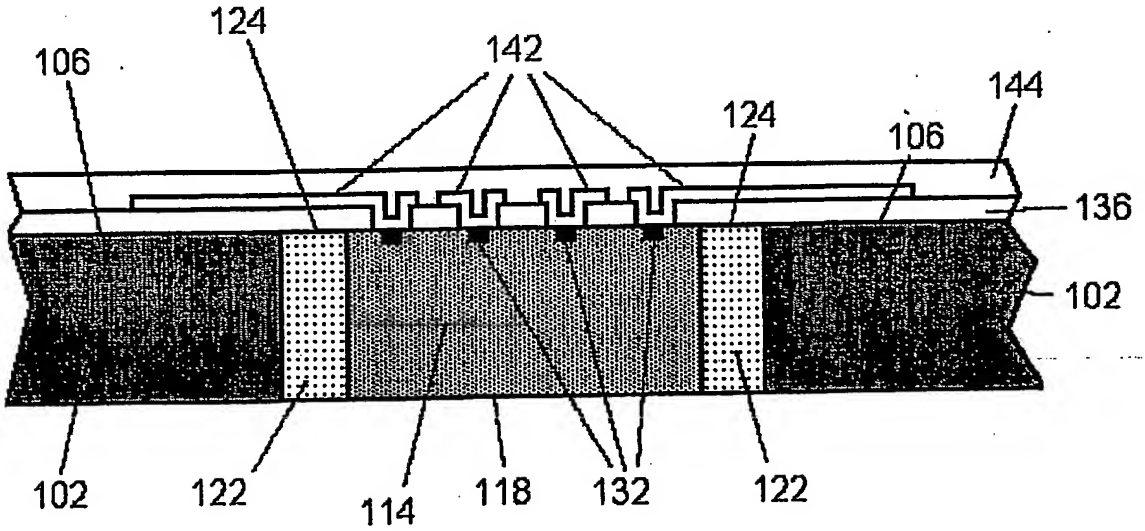


FIG. 12

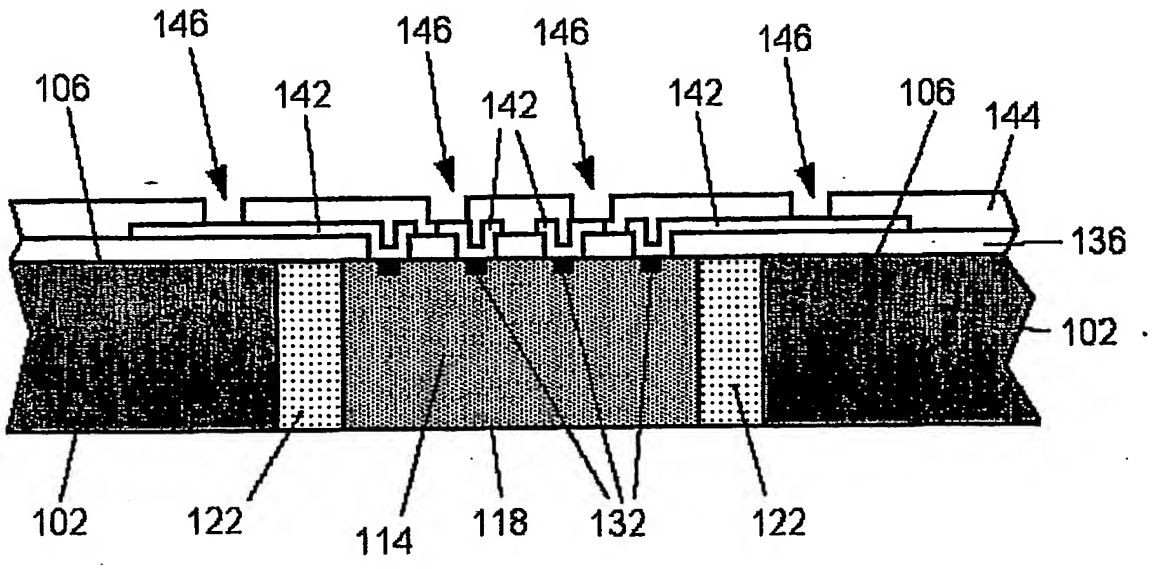


FIG. 13

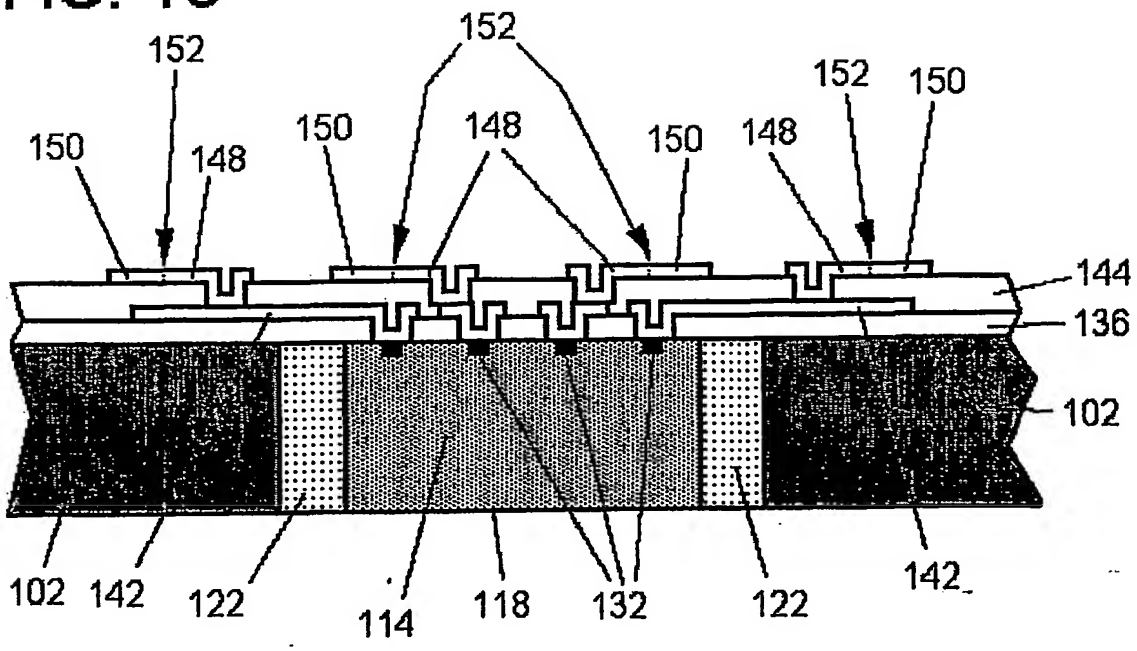


FIG. 14

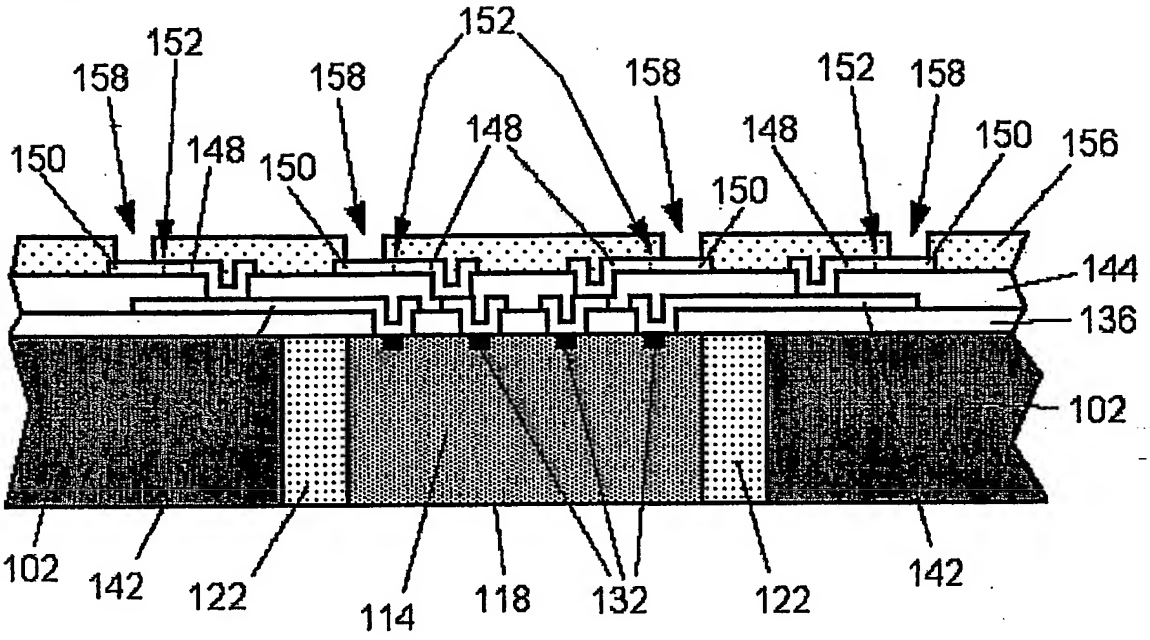


FIG. 15

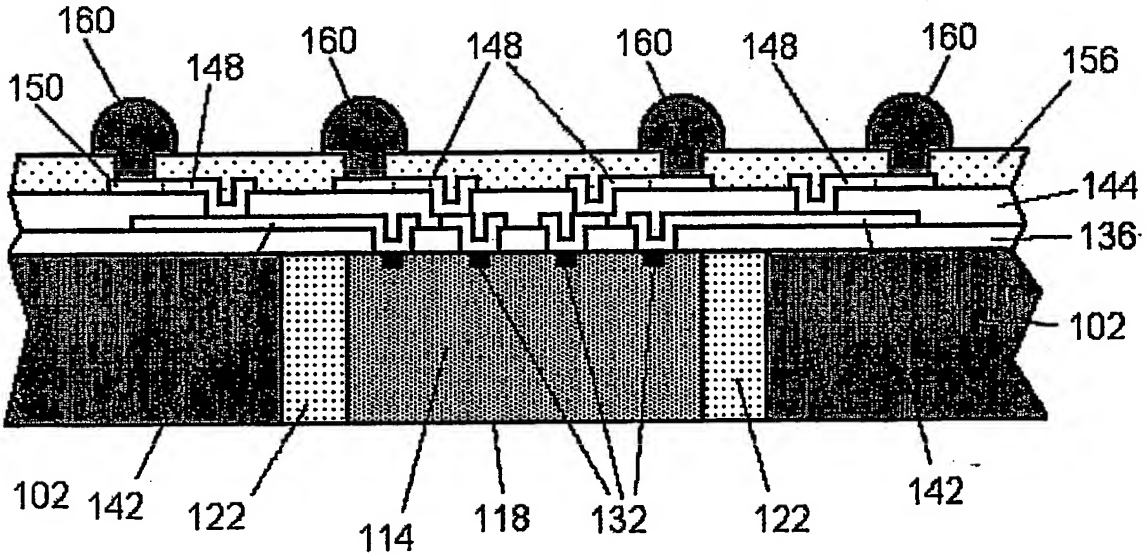


FIG. 16

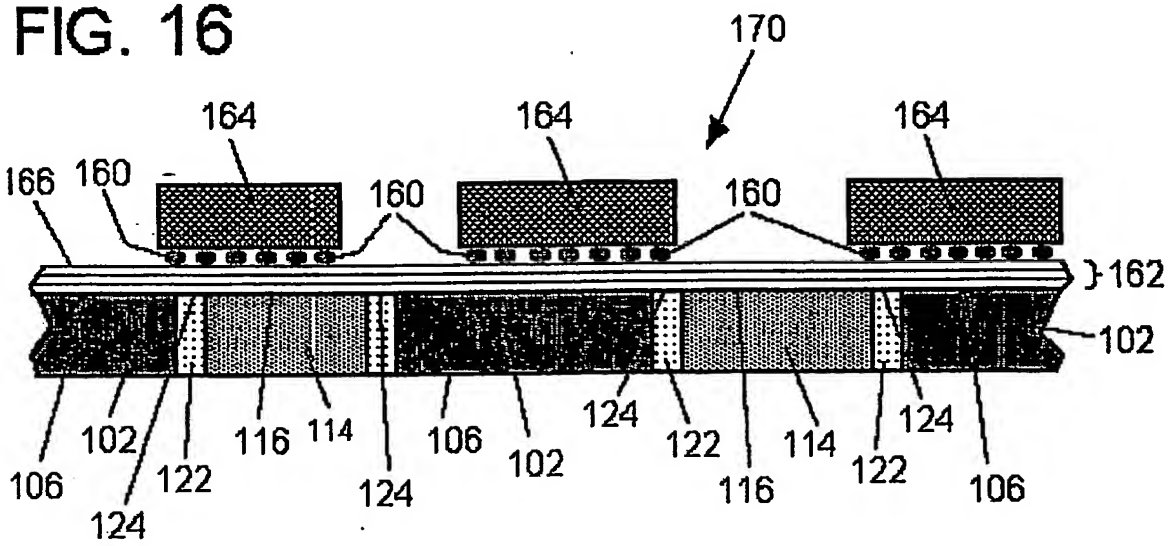


FIG. 17

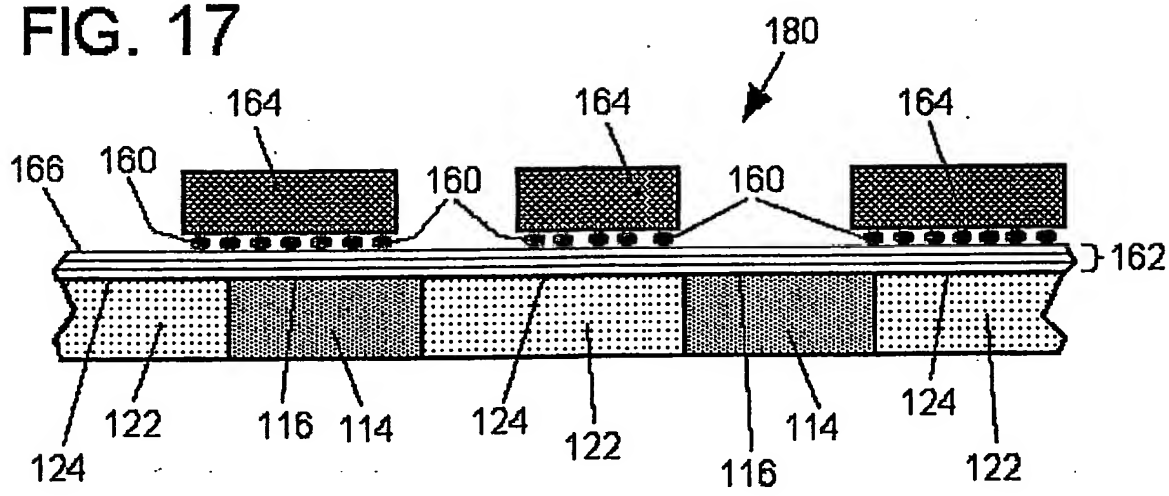


FIG. 18

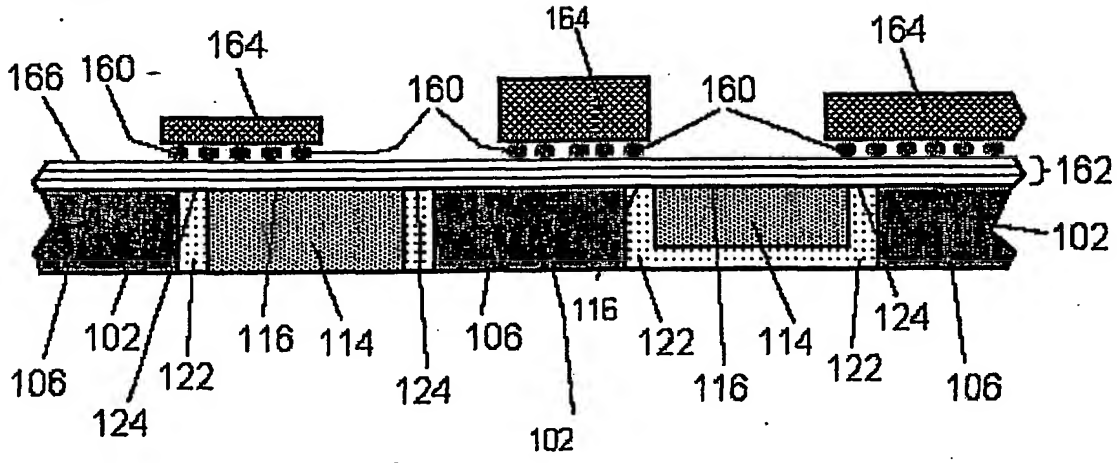


FIG. 19

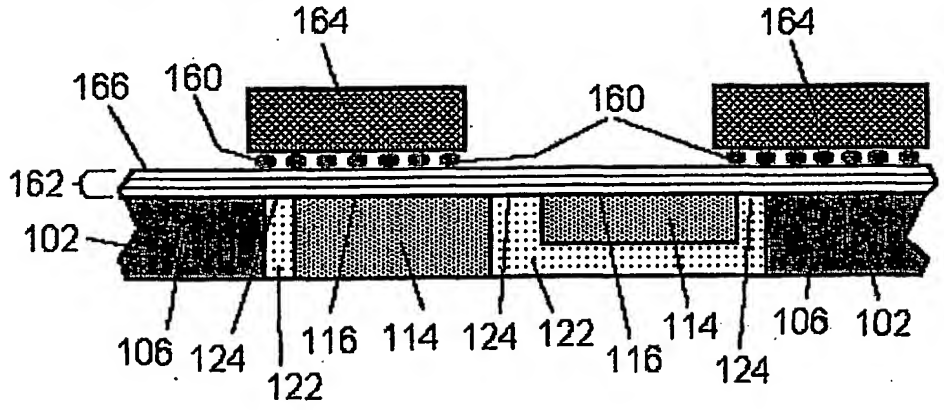


FIG. 20
Prior Art

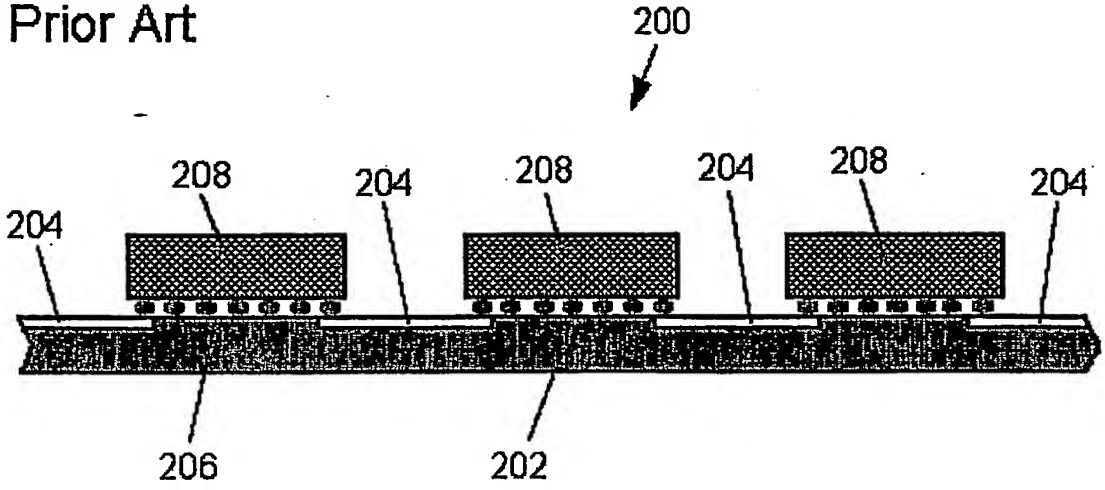
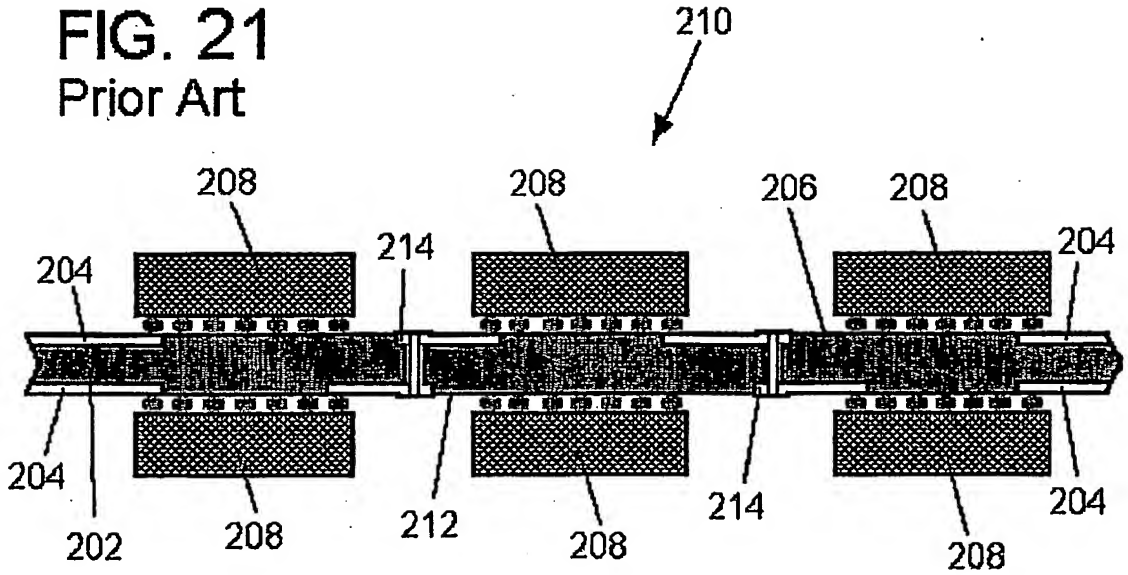


FIG. 21
Prior Art



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(74) Agent: STEFFEY, Charles, E.; Schwegman, Lundberg, Woessner & Kluth, P.O. Box 2938, Minneapolis, MN 55402 (US).

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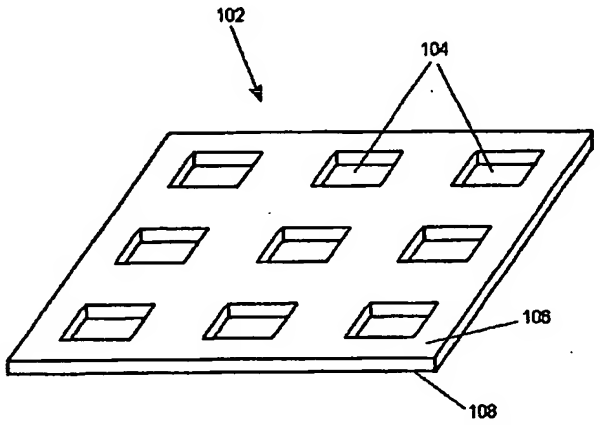
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
14 August 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MICROELECTRONIC SUBSTRATE WITH INTEGRATED DEVICES



(57) Abstract: A microelectronic substrate including at least one microelectronic die disposed within an opening in a microelectronic substrate core, wherein an encapsulation material is disposed within portions of the opening not occupied by the microelectronic dice, or a plurality microelectronic dice encapsulated without the microelectronic substrate core. Interconnection layers of dielectric materials and conductive traces are then fabricated on the microelectronic die, the encapsulation material, and the microelectronic substrate core (if present) to form the microelectronic substrate.

WO 02/033751 A3

INTERNATIONAL SEARCH REPORT

Inter ial Application No
PCT/US 01/31438

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/538

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 048 179 A (SHINDO MASAHIRO ET AL) 17 September 1991 (1991-09-17) abstract; figures 1,15-18	1-18, 21-28,31
A	column 1, line 35 -column 2, line 33 column 3, line 20 -column 8, line 53 claims 5-17	19,20, 29,30
X	US 5 998 859 A (HO CHUNG WEN ET AL) 7 December 1999 (1999-12-07) abstract; figures 1,2 column 4, line 35 -column 7, line 36 claims 1-4	1-15,21

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[X] Further documents are listed in the continuation of box C.

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7 May 2003	28/05/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Favre, P

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INTERNATIONAL SEARCH REPORT

Inter ıal Application No
PCT/US 01/31438

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 6 239 482 B1 (BURDICK JR WILLIAM EDWARD ET AL) 29 May 2001 (2001-05-29) abstract; figures 1-5,12,13 column 2, line 47 -column 4, line 3	1-21
A	claim 1	22-31

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INTERNATIONAL SEARCH REPORT

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Inter ...al Application No
PCT/US 01/31438

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